

What is claimed is:

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1. A computer system comprising:
 - a memory controller;
 - a main memory bus coupled to the memory controller; and
 - a synchronous non-volatile memory device coupled to the main memory bus.
2. The computer system of claim 1 wherein the synchronous non-volatile memory device has a command interface comprising:
 - a write enable connection (WE#) to receive a write enable signal;
 - a column address strobe connection (CAS#) to receive a column address strobe signal;
 - a row address strobe connection (RAS#) to receive a row address strobe signal;and
 - a chip select connection (CS#) to receive a chip select signal.
3. A synchronous flash memory device comprising:
 - an array of non-volatile memory cells; and
 - a plurality of external connections comprising,
 - a plurality of bi-directional data connections,
 - a plurality of memory address connections,
 - a clock input connection,
 - a write enable connection,
 - a column address strobe connection, and
 - a row address strobe connection.
4. The synchronous flash memory device of claim 3 wherein the plurality of external connections further comprises:
 - a clock enable connection,

11. A synchronous flash memory device comprising:
an array of non-volatile memory cells; and
a package having a plurality of interconnect pins arranged in a manner that corresponds to interconnect pins of a synchronous dynamic random access memory device, wherein the plurality of interconnect pins of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) interconnect pins of the synchronous dynamic random access memory.
12. The synchronous flash memory device of claim 11 wherein the plurality of interconnect pins comprises:
a plurality of bi-directional data connections,
a plurality of memory address connections,
a write enable connection,
a clock input connection,
a column address strobe connection,
a row address strobe connection, and
power supply connections.
13. The synchronous flash memory device of claim 12 wherein the plurality of interconnect pins further comprises:
a clock enable connection,
a chip select connection,
a plurality of memory array bank address connections,
a plurality of data mask connections,
a reset connection, and
a Vccp power supply connection.

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14. A synchronous flash memory device comprising:
an array of non-volatile memory cells; and
a package having a plurality of solder bump connections arranged in a manner that corresponds to solder bump connections of a synchronous dynamic random access memory device, wherein the plurality of solder bump connections of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) solder bump connections of the synchronous dynamic random access memory.
15. The synchronous flash memory device of claim 14 wherein the plurality of solder bump connections comprises:
a plurality of bi-directional data connections,
a plurality of memory address connections,
a write enable connection,
a clock input connection,
a column address strobe connection,
a row address strobe connection, and
power supply connections.
16. The synchronous flash memory device of claim 15 wherein the plurality of interconnect pins further comprises:
a clock enable connection,
a chip select connection,
a plurality of memory array bank address connections,
a plurality of data mask connections,
a reset connection, and
a Vccp power supply connection.

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17. A synchronous flash memory device having an interface comprising:
a clock input connection (CLK) to receive a clock signal;
a write enable connection (WE#) to receive a write enable signal;
a column address strobe connection (CAS#) to receive a column address strobe signal;
a row address strobe connection (RAS#) to receive a row address strobe signal;
a chip select connection (CS#) to receive a chip select signal;
a reset connection (RP#) to receive a reset signal; and
a Vccp power supply connection to receive an elevated power supply signal.
18. The synchronous flash memory device of claim 17 wherein the interface further comprises:
a plurality of bi-directional data connections (DQ);
a plurality of memory address connections;
a clock enable connection (CKE);
a plurality of memory array bank address connections (BA#);
power supply connections (Vcc and Vss); and
a plurality of data mask connections (DQM).
19. The synchronous flash memory device of claim 18 further comprising a package having a plurality of interconnect pins corresponding to the command interface connections.
20. The synchronous flash memory device of claim 19 wherein the interconnect pins are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

21. The synchronous flash memory device of claim 18 further comprising a package having a plurality of conductive interconnect locations corresponding to the command interface connections.

22. The synchronous flash memory device of claim 21 wherein the conductive interconnect locations are physically arranged in a pattern compatible with a synchronous dynamic random access memory (SDRAM).

23. A computer system comprising:

a memory controller;

a main memory bus coupled to the memory controller; and

a synchronous non-volatile flash memory device coupled to the main memory bus, wherein the synchronous non-volatile flash memory device has a command interface comprising:

a write enable connection (WE#) to receive a write enable signal;

a column address strobe connection (CAS#) to receive a column address strobe signal;

a row address strobe connection (RAS#) to receive a row address strobe signal;

and

a chip select connection (CS#) to receive a chip select signal.

24. The computer system of claim 23 wherein the synchronous non-volatile flash memory device comprises a package having a plurality of interconnect pins arranged in a manner that corresponds to interconnect pins of a synchronous dynamic random access memory device, wherein the plurality of interconnect pins of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) interconnect pins of the synchronous dynamic random access memory.

25. The computer system of claim 23 wherein the synchronous non-volatile flash memory device comprises a package having a plurality of solder bump connections arranged in a manner that corresponds to solder bump connections of a synchronous dynamic random access memory device, wherein the plurality of solder bump connections of the synchronous flash memory device comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) solder bump connections of the synchronous dynamic random access memory.

26. The computer system of claim 23 wherein the synchronous non-volatile flash memory device comprises a plurality of external connections comprising:

- a plurality of bi-directional data connections;
- a plurality of memory address connections;
- a clock input connection;
- a clock enable connection;
- a plurality of memory array bank address connections;
- power supply connections;
- a plurality of data mask connections;
- a reset connection; and
- a Vccp power supply connection.

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